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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,578	07/16/2003	Akinori Shibayama	60188-580	7089

7590 12/29/2004

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EXAMINER	
LAM, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,578	SHIBAYAMA, AKINORI	
	Examiner	Art Unit	
	David Lam	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6* is/are rejected.

7)☒ Claim(s) *5 and 7-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakayama et al. (6,430,103).

Regarding to claims 1, 3, Nakayama et al. disclose a semiconductor integrated circuit comprising: a memory (51); a plurality of logic portions (50-1, 50-2) that are connectable to the memory and respectively carry out data processing; a separation portion (55) that connects at least on of the plurality of logic portions to the memory while separating the other logic portions from the memory, wherein the plurality of logic portions have the same function; and of the plurality of portions, the separation portion connects to the memory a logic portion that has integrity. *See Fig. 15; Cols. 14-15.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. (6,430,103) in view of Takashimizu et al. (2002/0112075).

Nakayama et al. disclose the claimed invention as note above but lack an inclusion of wherein the plurality of logic portions have different function, and the separation portion connects a logic portion that has a function required by the semiconductor integrated circuit to the memory.

However, Takashimizu et al. disclose a semiconductor integrated circuit comprising: pluralities of logic portions have different function (10-1, 10-2), and the separation portion connects a logic portion that has a function required by the semiconductor integrated circuit to the memory. *See Figs. 5-8; Pages 4-6.*

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Nakayama et al.'s logic portion by utilizing Takashimizu et al.'s logic portions to provide an efficiency, high-speed network system in a semiconductor memory device.

3. Claims 4, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. (6,430,103) in view of Cutter et al. (6,128,240).

As per above discussion, Nakayama et al. disclose the claimed invention but lack an inclusion of wherein the separation portion comprises a plurality of fuse/antifuse circuits

arranged between the memory and the respectively plurality of logic portion and a fuse of the fuse circuits that corresponds to the others portion is severed/antifuse of the antifuse circuits that corresponds to one of the logic portions is in a conductive state, while another antifuse of the antifuse circuits that corresponds to the other portion(s) is in a non-conductive state.

However, Cutter et al. disclose a plurality of fuse/antifuse circuits (76) that operated as a switching circuits/separation portion to connecting/separating by conducting/non-conducting a memory device to a plurality of signal lines. *See. Figs. 1-5; Cols. 3-6.*

It would have been obvious to one having ordinary skill in the art at the time of the invention to modify Nakayama et al.'s switching circuit/separation portion by utilizing Cutter et al.' fuse/antifuse circuits to provide reliable, high-speed signals processing with in a semiconductor memory device.

Allowable Subject Matter

4. Claims 5, 7-15, 16-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach the above noted semiconductor integrated circuit and further comprising a power source separation circuit that separates the logic portion that is in a separated state from the power source supplied to the logic portion, and others as claimed in claims 7, 17, 18.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam

December 27, 2004

DAVID LAM
PRIMARY EXAMINER